Matrox RadientPro CL >>

Full-featured Camera Link[®] frame grabber with FPGA-based processing offload

Benefits

Capture images at the highest Camera Link rates with support for the Full and 80-bit modes at up to 85MHz (single-Full model).

Eliminate lost pixels through a PCle[®] 2.0 x8 host interface and ample on-board buffering.

Reduce cabling and eliminate power supplies by way of Power over Camera Link (PoCL) support.

Offload and accelerate image processing to free and assist the host CPU using an Altera® Stratix® V FPGA.

Simplify the development of custom on-board image processing using the optional Matrox FPGA Development Kit (FDK).

Reduce development and validation costs through a managed lifecycle offering consistent long term availability.

Implement image capture with ease and confidence using Matrox Imaging Library (MIL) application development toolkit.

Maintain flexibility and choice by way 64-bit Windows 7/8.1/10, Linux $^{\otimes 1}$ and RTX64¹ (RTOS) support.

Full-featured Camera Link vision processor

The Matrox RadientPro CL is a vision processor board capable of handling the highest image acquisition rates supported by the Camera Link interface standard, specifically the Full and 80-bit modes (single-Full model). The Matrox RadientPro CL also makes available a FPGA device capable of offloading the host system from having to deal with repetitive compute-intensive image processing algorithms that consume substantial host system bandwidth. This FPGA device can be tailored for specific algorithms either by Matrox or by using the optional Matrox FPGA Development Kit (FDK).

Offload and accelerate repetitive tasks from the host CPU

As image size continues to grow, frame rate steadily increases, and applications are expected to do more, the demands on the host system keep rising. The Matrox RadientPro CL can lessen the pressure by offloading repetitive compute-intensive image processing operations using the on-board Altera Stratix V FPGA, freeing valuable processing resources for the rest of the application and even accelerating the application. Candidate operations include spatial and temporal filtering, gain and offset correction, dead pixel correction, optical and perspective distortion correction, Bayer color interpolation, color space conversions, and frequency domain transformations. The operations performed on-board are controlled through the Matrox Imaging Library (MIL) application development software. Through MIL, a FPGA configuration can be rearranged to perform a required sequence of operations without having to necessarily generate a new FPGA configuration. When the need arises, Matrox's FPGA design services can be employed to generate an application-specific FPGA configuration. Users can also use the Matrox FDK to create custom FPGA configurations.

Versatile Camera Link interface

For low-latency and deterministic acquisition, Camera Link provides a scalable and proven solution for vision applications. From cost-sensitive, low data rate applications, to mainstream applications including color, and right up to maximum bandwidth applications, Camera Link is an excellent fit.



Versatile Camera Link interface (cont.)

The use of the mini Camera Link connector (HDR) on the RadientPro CL facilitates higher density multi-camera system designs by enabling two Base or one Full mode Camera Link interface with triggering and general purpose I/O in a single slot

The Matrox RadientPro CL (single-Full model) supports the latest area and line scan cameras up to the Camera Link Full and 80-bit modes at 85MHz. When interfaced to PoCL enabled cameras, overall cabling complexity is reduced by eliminating the need for bulky and costly external camera power supplies.

High-performance host interface

An PCIe[®] 2.0 x8 host interface provides the throughput necessary to ensure the continuous flow of pixels from the Matrox RadientPro CL to host memory. With a peak bandwidth of up to 4 GB/s, the Matrox RadientPro CL's host interface prevents pixels from inadvertently being discarded while the point-to-point connectivity of PCIe stops other add-in devices from taking away valuable bandwidth between the frame grabber and the host PC.

Lifecycle managed for consistent long term supply

Matrox RadientPro CL block diagram

Matrox Imaging not only carefully selected each component in the Matrox RadientPro CL to ensure product availability in excess of five years, but also exercised strict change control to provide consistent supply. Longevity of stable supply lets OEMs achieve maximum return on the original investment without incurring the additional costs associated with the repeated validation due to constantly-changing products.

Field-proven application development software

Matrox RadientPro CL is supported by Matrox Imaging Library (MIL), a comprehensive collection of software tools for developing industrial imaging applications. MIL features interactive software and programming functions for image capture, processing, analysis, annotation, display and archiving. These tools are designed to enhance productivity, thereby reducing the time and effort required to bring your solution to market. Refer to the MIL datasheet for more information.

Included with MIL are ready-made configurations for the FPGAbased processing core that implement a variety of image processing functions. Custom configurations can also be created by Matrox experts on demand and upon evaluation. For developers seeking to create their own image processing functions, the Matrox FDK is also available. It provides a component library and tools to enable creation of custom FPGA configurations for the Matrox RadientPro CL. Refer to the Matrox FDK datasheet for more information.



Specifications

Hardware

- PCIe[®] 2.0 x8 host bus interface
- Altera Stratix V 340K LE FPGA device
 - for Matrox or custom image processing algorithms designed with Matrox FDK
- 2 GB of DDR3-1600 SDRAM
- 0/16/32 MB of QDR2 SRAM
- Camera Link[®] 2.0 acquisition
 - Mini Camera Link connectors (HDR-26)
 - Power over Camera Link with SafePower
 - 20 to 85 MHz Camera Link clock
 - One (1) Medium/Full Camera Link port (single-Full model)
 - Support for 8-tap x 10-bit and 10-tap x 8-bit (80-bit) modes
 - Two (2) Base Camera Link ports (dual-Base model)
- Supports frame and line scan sources
- On-board image reconstruction
- On-board color space conversion
- Input formats
 - Mono/Bayer 8-bit and 16-bit
 - BGR packed 24-bit and 48-bit
- Output formats
 - Mono 8-bit and 16-bit
 - 24-bit BGR/RGB packed
 - 32/48-bit BGRa/RGBa
 - YUV 16-bit
 - YCrCb
- One (1) DBHD-15 male GPIO connector
 - Three (3) TTL configurable auxiliary I/O's
 - Two (2) LVDS auxiliary inputs
 - One (1) LVDS auxiliary output
 - Two (2) opto-isolated auxiliary inputs
- Optional add-on DBHD-15 male GPIO connector
 - Three (3) TTL configurable auxiliary I/O's
 - Two (2) LVDS auxiliary inputs
 - One (1) LVDS auxiliary output
 - Two (2) opto-isolated auxiliary inputs
- Support for one (1) quadrature rotary encoder
- per Camera Link[®] portMIL license fingerprint and storage

Specifications (Cont.)

Dimensions and environmental information

- Matrox RadientPro CL
- 167.6 mm L x 111.1 mm H x 18.7 mm W (6.6" x 4.38" x 0.74")
- Operating temperature: 0 to 40 $^{\circ}\text{C}$ (32 to 104 $^{\circ}\text{F})$
- Relative humidity: up to 95% (non-condensing)
- FCC class A
- CE class A
- RoHS-compliant

Software

- Matrox Imaging Library (MIL) drivers for 64-bit Windows 7/8.1/10
- MIL drivers for 64-bit Linux¹
- Implements GenICam[™] 2.3.1 (CLProtocol 1.1) and GenICam GenCP 1.0 under Windows/Linux
- MIL drivers for RTX64¹
- Optional Matrox FDK for use with Impulse CoDeveloper and Altera Quartus[®] II

Ordering Information

| Hardware | |
|------------------|--|
| Part number & De | scription |
| RP2GDB340300* | Matrox RadientPro dual-Base Camera Link® PCle® 2.0 x8 frame grabber with 2 GB DDR3 SDRAM, Altera Stratix V 5SGXA3 FPGA and no SRAM |
| RP2GSF340300* | Matrox RadientPro single-Medium/Full Camera Link® PCIe® 2.0 x8 frame grabber with 2 GB DDR3 SDRAM, Altera Stratix V 5SGXA3 FPGA and no SRAM |

Notes: 1. Ask for availability

Corporate headquarters:

Matrox Electronic Systems Ltd. 1055 St. Regis Blvd. Dorval, Quebec H9P 2T4 Canada Tel: +1 (514) 685-2630 Fax: +1 (514) 822-6273

For more information, please call: 1-800-804-6243 (toll free in North America) or (514) 822-6020 or e-mail: imaging.info@matrox.com or http://www.matrox.com/imaging



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